AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning at page 3, line, 1, with the following amended paragraph:

The data driver 18 selects reference voltages in accordance with the input data in response to control signals from the timing controller 12 to convert the same into an analog image signal and applies the converted signal to a liquid crystal panel 22. The gate driver 20 performs an on/off control of gate terminals of thin film transistors (TFTs) 23 (i.e., switching devices) arranged on the liquid crystal panel 22, one scan line 24 ~~by one line~~ at a time, in response to the control signals input from the timing controller 12. Also, the gate driver 20 allows the analog image signals from the data driver 18 to be applied to each pixel connected to each TFT 23 via a data line 25.

Please replace the paragraph beginning at page 3, line, 34, with the following amended paragraph:

In order to achieve these and other objects of the invention, a liquid crystal display device according to one aspect of the present invention includes a timing controller for receiving control signals transmitted from a host system; a frequency detector connected to either an input terminal or an output terminal of the timing controller to detect the transmitted control signals; compensation voltage setting means for compensating the driving voltage in response to the control signals detected from the frequency detector so as to assure a charge time of each thin film transistor; and a ~~digital to digital~~ voltage converter for generating a compensation voltage set by the compensation voltage setting means to deliver the compensation voltage to a liquid crystal display panel.

Please replace the paragraph beginning at page 4, line, 34, with the following amended paragraph:

Fig. 3 is a block diagram of a driving circuit for a liquid crystal display device according to a first embodiment. The interface, the timing controller, the ~~digital to digital~~ voltage converter and the liquid crystal display panel in Fig. 3 are identical to those of the driving circuit in Fig. 1. Therefore, said elements in Fig. 3 are given by the same reference numerals as those in Fig. 1.

Please replace the paragraph beginning at page 5, line, 1, with the following amended paragraph:

Referring to Fig. 3, the liquid crystal display device according to the first embodiment includes an interface 10 for receiving and transferring data (e.g., RGB data) and control signals (e.g., an input clock, a horizontal synchronizing signal, a vertical synchronizing signal and a data enable signal) input from a driving system such as a personal computer, a timing controller 12 for generating control signals for driving a data driver 18 consisting of a plurality of data driving ICs (not shown) and a gate driver 20 consisting of a plurality of gate driving ICs (not shown) using the control signals input via the interface 10, a frequency detector 30 for detecting frequencies of the control signals output to the output terminal of the timing controller 12, a compensation voltage setting part 32 for retrieving and comparing the frequencies detected from the frequency detector 30 to generate a control signal for setting a compensation voltage according to said frequencies, a ~~digital to digital~~ voltage converter 34 for generating a desired gate high voltage Vgh for raising and lowering a reference voltage Vin from the interface 10 using the control signal from the compensation voltage setting part 32 to deliver the same to the gate driver, and a liquid crystal display panel 22 driven with the gate high voltage Vgh and a data signal applied from the gate driver 20 and the data driver 18, respectively.

Please replace the paragraph beginning at page 5, line, 14, with the following amended paragraph:

The frequency detector 30 receives the control signals (e.g., a vertical synchronizing signal and a data signal) from the timing controller 12 via an output transmission line of the timing controller 12 and sends them to the compensation voltage setting part 32. The

compensation voltage setting part 32 retrieves the control signals from the frequency detector 30, and generates a control signal for setting a compensation voltage for the gate high voltage Vgh so as to sufficiently drive the TFTs provided within the liquid crystal display panel 22 in response to the retrieved control signals to deliver the same to the ~~digital to digital~~ voltage converter 34. The ~~digital to digital~~ voltage converter 34 raises or lowers a reference voltage Vin from the interface 10 by the control signal from the compensation voltage setting part 32 to generate a compensation voltage sufficient to drive the TFTs, and delivers the compensation voltage to the liquid crystal display panel 22.

Please replace the paragraph beginning at page 6, line, 6, with the following amended paragraph:

Fig. 6 is a block diagram of a driving circuit for a liquid crystal display device according to a third embodiment. The driving circuit in Fig. 6 has the same driving characteristic as that in Fig. 3. except that the compensation voltage setting part sets a compensation voltage for compensating for a common voltage Vcom and the ~~digital to digital~~ voltage converter generates the compensation voltage set by the compensation voltage setting part to apply it to the liquid crystal display panel. Therefore, only the compensation voltage setting part and the ~~digital~~ DC to ~~digital~~ DC converter being different from those in Fig. 3 will be described.

Please replace the paragraph beginning at page 6, line, 12, with the following amended paragraph:

As shown in Fig. 6, the compensation voltage setting part [[36]] 32 retrieves control signals from the frequency detector 30, and generates a control signal for setting a compensation voltage for a common voltage Vcom so as to sufficiently drive the TFTs provided within the liquid crystal display panel 22 in response to the retrieved control signals to deliver the same to ~~digital to digital~~ voltage converter 38. The ~~digital to digital~~ voltage converter 38 raises or lowers a reference voltage Vin from the interface 10 by the control signal from the compensation

voltage setting part 32 to generate a compensation voltage sufficient to drive the TFTs, and delivers the compensation voltage to the liquid crystal display panel 22.

Please replace the paragraph beginning at page 6, line, 32, with the following amended paragraph:

In order to solve this problem, the frequency detector 30 as shown in Fig. 6 or Fig. 7 detects the control signals input to, or output from, the timing controller 12 and delivers the detected control signals to the compensation voltage setting part [[36]] 32. The compensation voltage setting part [[36]] 32 sets an appropriate compensation voltage so that the TFT can obtain an optimum charge rate as shown in Fig. 8. In this case, the charge rate of the TFT is compensated by decreasing the common voltage Vcom to 3V. In other words, the common voltage Vcom is reduced to lengthen a region Ct3. Accordingly, the charged region Ct3 of the TFT is sufficiently lengthened, so that an optimum charge rate can be obtained.

Please replace the paragraph beginning at page 7, line, 1, with the following amended paragraph:

Fig. 9 is a block diagram of a driving circuit for a liquid crystal display device according to a fifth embodiment of the present invention. The driving circuit in Fig. 9 has the same driving characteristic as that in Fig. 3 or Fig. 6, except that the compensation voltage setting part sets a compensation voltage for compensating for a gate high voltage Vgh and a common voltage Vcom and the ~~digital to digital~~ voltage converter generates the compensation voltage set by the compensation voltage setting part to apply it to the liquid crystal display panel. Therefore, only the compensation voltage setting part and the ~~digital to digital~~ voltage converter being different from those in Fig. 3 or Fig. 6 will be described.

Please replace the paragraph beginning at page 7, line, 8, with the following amended paragraph:

As shown in Fig. 9, the compensation voltage setting part [[40]] 32 retrieves control signals from the frequency detector 30, and generates a control signal for setting a compensation voltage for a gate high voltage Vgh and a common voltage Vcom so as to sufficiently drive the TFTs provided within the liquid crystal display panel 22 in response to the retrieved control signals to deliver the same to a ~~digital-to-digital~~ voltage converter 42. The ~~digital-to-digital~~ voltage converter 42 heightens and/or lowers a reference voltage Vin from the interface 10 by the control signal from the compensation voltage setting part [[40]] 32 to generate a compensation voltage enough to drive the TFTs, and delivers the compensation voltage to the liquid crystal display panel 22.

Please replace the paragraph beginning at page 7, line, 29, with the following amended paragraph:

In order to solve this problem, the frequency detector 30 as shown in Fig. 9 or Fig. 10 detects the control signals input to or output from the timing controller 12 and delivers the detected control signals to the compensation voltage setting part [[40]] 32. The compensation voltage setting part [[40]] 32 sets an appropriate compensation voltage so that the TFT can obtain an optimum charge rate as shown in Fig. 11. In this case, the charge rate of the TFT is compensated by resetting the gate high voltage Vgh to 19V and the common voltage Vcom to 3V. In other words, the gate high voltage Vgh is heightened while the common voltage Vgh is lowered to lengthen a charged region Ct4. Accordingly, the charged region Ct4 of the TFT is sufficiently lengthened, so that an optimum charge rate can be obtained.